WHAT IS CLAIMED IS:

1. A channel associated signaling (CAS) data processing apparatus of an STM-1 interface block, comprising:

a plurality of framers, each configured to receive a signaling data stream from at least one communication circuit link;

a CAS signaling processor, coupled to receive a start signal from a CPU and the signaling data stream from each of the framers, and reformat the signaling data streams into a prescribed format; and

a common memory (CM) coupled to receive and store the formatted data outputted from the CAS signaling processing unit.

2. The apparatus of claim 1, wherein the CAS signaling processing unit outputs a busy signal to the CPU upon receiving the start signal, and maintains the busy signal until the data streams from each of the framers has been processed.

3. The apparatus of claim 2, wherein the CAS signaling processing unit ignores the start signal outputted from the CPU when the busy signal is maintained.

4. The apparatus of claim 1, wherein the CAS signaling processor comprises:

a stream selector coupled to receive the signaling data streams synchronized with a system clock from the plurality of framers, and output an ordered signaling data bit stream;

a signaling processing unit, coupled to receive and store the data bit stream outputted from the stream selector, and convert the received data into a report format;

a CPU interface to provide an interface between the CPU and the signaling processing unit; and

an address generation circuit to generate a write address of the CM in accordance with an address increase signal outputted from the signaling processing unit.

5. The apparatus of claim 4, wherein the CAS signaling processor reads a prescribed number of time slots from the signaling data stream in accordance with a read clock signal and reformats the data into the report format.

6. The apparatus of claim 5, wherein one cycle of the read clock signal is equivalent to an interval of one time slot.

7. The apparatus of claim 4, wherein the CPU interface receives the start signal from the CPU and generates a control signal that activates the stream selector, the

signaling processing unit, and the address generation circuit, and wherein the CPU interface outputs a busy signal to the CPU until the signaling processing unit has converted all of the received data into the report format.

8. The apparatus of claim 4, wherein the signaling processing unit outputs a link number increase signal (LNIS) to the stream selector when the processing for one link is finished, and receives the signaling data stream for the next link from the stream selector in response to the LNIS.

9. The apparatus of claim 4, wherein the address generation unit increases the write address of the CM in response to an address control signal from the signaling processing unit when the CM access is finished.

10. A channel associated signaling (CAS) data processing apparatus of a STM-1 interface block, comprising:

a plurality of framers, coupled to extract signaling data streams from a plurality of E1 links;

a CPU, configured to output a start signal to control signaling data processing;

a signaling processing unit, which is activated by the start signal to reformat the signaling data streams inputted from the plurality of framers and output report data in an order of each link;

a CPU, interface which interfaces the CPU and the signaling processing unit; and

a common memory (CM) interface, which interfaces the CAS signaling processing unit with a common memory to provide the report data to the common memory.

11. The apparatus of claim 10, wherein a number of E1 links is 21, and the CPU interface activates the signaling processing unit in response to the start signal.

12. The apparatus of claim 10, wherein the CPU interface outputs a busy signal to the CPU during signaling data processing by the signaling processing unit, and wherein the start signal outputted from the CPU is ignored during when the busy signal is outputted.

13. The apparatus of claim 10, wherein the signaling processing unit comprises:

a stream selector coupled to receive the signaling data streams synchronized with a system clock from the plurality of the framers and to output an ordered signaling data stream; and

a signaling processor coupled to receive the ordered signaling data streams from the stream selector and to reformat the ordered signaling data into a prescribed number of time slot report data.

14. The apparatus of claim 13, wherein one cycle of the clock signal is equivalent to an interval of one time slot.

15. The apparatus of claim 13, wherein the CM interface increases the write address of the CM in accordance with an address increase signal of the signaling processor when the CM access is finished.

16. A data processing apparatus for a STM-1 interface block, comprising:

a plurality of framers, configured to interface 21 E1 links and extract signaling data streams from the E1 links;

a CAS signaling processing unit, which reformats the signaling data streams outputted from the plurality of framers into report data in link order;

a common memory (CM) coupled to store the report data outputted from the CAS signaling processing unit;

a stream select unit which outputs the inputted signaling data streams in a prescribed order in accordance with a link increase signal outputted from the CAS signaling processing unit;

a signaling processing unit which reads the bit stream outputted from the stream select unit and reformats it into the report format;

a CPU coupled to output a start signal to the CAS signaling processing unit to initiate CAS signaling data processing;

a CPU interface which interfaces the CPU and the signaling processing unit; and

an address generation unit which generates a write address of the CM in a prescribed order in accordance with the address increase signal outputted from the CAS signaling processing unit.

17. The apparatus of claim 16, wherein the signaling processing unit outputs the busy signal to the CPU during signaling data processing, and the start signal is ignored when the busy signal is outputted.

18. The apparatus of claim 16, wherein the CAS signaling processing unit reads each channel data from the signaling data stream in accordance with a read clock signal and reformats the channel data into the report data when a 4 time slot read is completed.

19. The apparatus of claim 18, wherein one cycle of the read clock signal is equivalent to an interval of one time slot.

20. The apparatus of claim 16, wherein the signaling processing unit outputs a link number increase signal to the stream select unit when processing of one link is completed, and then receives the signaling data stream of the next link.

21. The apparatus of claim 1, wherein the communication circuit links comprise one of E1 links and T1 links, and wherein each one of the plurality of framers the signaling data stream from the a corresponding link.

22. The apparatus of claim 1, wherein the plurality of links comprises 21 links.

23. The apparatus of claim 13, wherein the prescribed number of time slots is 4.

24. A channel associated signaling processing unit, comprising:

a stream selector, coupled to receive a data stream from a communications channel link;

a signaling processing unit, coupled to receive an output of the stream selector and output it in a prescribed format; and

a controller, coupled to provide a control signal to the to the stream selector and the signaling processing unit, and generate a write address signal to control a storage of an output of the signaling processing unit.

25. The device of claim 24, wherein the controller comprises:

a CPU interface, configured to receive a start signal from a CPU, output a busy signal to the CPU when the signaling processing unit is processing the output of the stream selector, and output the control signal to the to the stream selector and the signaling processing unit, and

an address generator, coupled to receive an address increase signal from the signaling processing unit and the control signal and output the write address signal.

26. The device of claim 24, wherein the stream selector is configured to extract signaling data streams from a plurality of E1 links through a corresponding plurality of framers.

27. The device of claim 24, wherein the signaling processing unit provides a link number increase signal (LNIS) to the stream selector when the processing for one channel link is finished, and receives a signaling data stream for the next channel link from the stream selector in response to the LNIS.

28. The device of claim 24, further comprising a plurality of framers, coupled to provide the data stream to the stream selector, a CPU interface, configured to receive a start signal from a CPU and generate the control signal, and a common memory, coupled to receive the write address signal and store the formatted data outputted by the signaling processing unit.